Jiahao Lin

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Summary

I am a PhD candidate in Electrical and Computer Engineering at the University of Wisconsin–Madison, advised by Prof. Umit Y. Ogras. Research interests include computer architecture, reconfigurable systems, and dynamic scheduling for data-intensive workloads, with applications in RF autonomy and hybrid LLM services.

Education

Shanghai JiaoTong University, BS in Micro-Electronics 2017 – 2021

University of Wisconsin-Madison, MS in Electrical and Computer Engineering 2022 – 2024

University of Wisconsin-Madison, PhD in Electrical and Computer Engineering 2024 – 2027

Experience

FPGA and RISC-V Intern, Analog Devices, Inc – Full-time – Shanghai, China Aug 2021 – Aug 2022

- DUT verification and embedded software testing for the Bluetooth RF module in an audio processing system
- Set up an emulation framework for PMIC and battery management systems on FPGA and FMC boards.
- Integrated a debug module for RISC-V IP using JTAG and on-chip debugging tools.

Projects

High-level Simulator and DSE framework for Reconfigurable and Chiplet-based Systems

- Developed high-level simulators and design space exploration (DSE) frameworks for reconfigurable and chiplet-based systems
- Conducted architectural studies of reconfigurable systems for wideband spectrum sensing applications
- Evaluated chiplet-based architectures for hybrid LLM services, analyzing the impact of chiplet placement, chiplet selection, task mapping, and request batching
- Supported DSE and trade-off analysis to enable hardware-software-communication co-design

Real-time Dynamic Scheduler of Reconfigurable Systems for Real-time Large-volume Processing

- Developed a communication-aware dynamic scheduling approach that integrates work-steal and preloading mechanisms for throughput and real-time requirements

Resource Management for Heterogeneous Antenna Arrays and Dynamic Spectrum Access

- Designed agents, including the Reinforcement Learning and Heuristic agents on the simulator, with the generation of pulse-descriptor words from complex RF environments
- Adapted the inference and fine-tuning of intelligent agents to a fine-grained and realistic RF spectral environment

Power Model for Heterogeneous SoC CEDR

- Built runtime power model for big, little cores and reconfigurable array-based accelerators, integrated within a runtime compilation framework
- Employed performance counters to build regression-based power models for CPUs. Estimate accelerator kernel power consumption through instruction-level power profiling

SoC design for video and internet applications

- Got the first prize in the national contest. Responsible for memory sub-system design, embedded software, Lwip integration, and demo on QT software.

Publications

CADAS: Communication-Aware Dynamic Scheduler on CGRAs for Large-volume and Real-time Processing
Jiahao Lin,H. Umut Suluhan,Chaitali Chakrabarti,Ali Akoglu,and Umit Ogras

ACM TECS (2026)
DUET: Disaggregated Hybrid Mamba-Transformer LLMs with Prefill and Decode-Specific Packages
Alish Kanani,Sangwan Lee,Han Lyu,Jiahao Lin,Jaehyun Park,and Umit Ogras

DAC (2026)
An Overview of Challenges and Requirements for Real-Time Spectrum Sensing in Modern RF Autonomy Systems
Jiahao Lin, and et al.

IEEE Design & Test (2025)
K-PACT: Kernel Planning for Adaptive Context Switching-A Framework for Clustering, Placement, and Prefetching in Spectrum Sensing.
H. Umut Suluhan, Jiahao Lin,Serhan Gener,Chaitali Chakrabarti,Umit Ogras,and Ali Akoglu

ICCAD (2025)
Reconfigurable System Design and Trade Studies for Dynamic Spectral Sensing.
Arindam Dutta,Jiahao Lin,H. Umut Suluhan,Gerard Gubash,Ali Akoglu,and et al.

Asilomar (2025)
eMamba: Efficient Acceleration Framework for Mamba Models in Edge Computing.
Kim Jiyong,Jaeho Lee,Jiahao Lin,Alish Kanani,Miao Sun,Umit Ogras,and Jaehyun Park

ESWEEK (2025)

Technologies

Languages: System Verilog, Python, C++, C, HTML, JavaScript, TCL, Shell

Tools: Xilinx, Cadence and Synopsys toolchain, QT, OpenOCD